



# UNITED STATES PATENT AND TRADEMARK OFFICE

MW

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,158	08/28/2001	William R. Wheeler	10559-596001 / P12880	4619
20985	7590	01/08/2004		
FISH & RICHARDSON, PC 12390 EL CAMINO REAL SAN DIEGO, CA 92130-2081			EXAMINER WHITMORE, STACY	
			ART UNIT	PAPER NUMBER
			2812	

DATE MAILED: 01/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/941,158

Applicant(s)

WHEELER ET AL.

Examiner

Stacy A Whitmore

Art Unit

2812

MW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 29 September 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-5,7-9 and 11-28 is/are pending in the application.
- 4a) Of the above claim(s) 26-28 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5,7-9 and 11-25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 August 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.  
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 12. 6) ☐ Other: \_\_\_\_\_

FINAL ACTION

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
2. Claims 1-5, 7-9, 11, 14-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US Patent 6,366,874) in view of Parson (US Patent 6,053,947).
3. As for claims 1-5, 7-9, 11, and 14-23, Lee disclosed the invention substantially as claimed, including a method (system, computer program product, and processor and memory) for designing a logic circuit comprising:
  - generating a functional design (model) of a logic circuit by selecting, placing, and connecting reusable graphical library elements using a graphical user interface (GUI), the graphical library elements representing logical functions and connections between the logical functions [col. 2, line 58 – col. 3, lines 12];
  - refining the functional design (model) to represent a hardware design (functional design) of the logic circuit using the GUI [col. 3, lines 32-35];
  - maintaining a (descriptive netlist) data structure representative of a model, the model including combinational blocks, state elements, and graphical library elements of the logic circuit [col. 2, lines 45-46, col. 3, lines 32-39, and 60-67, and col. 4, lines 1-2];
  - the model including combinational blocks, state elements and graphical library elements of the logic circuit [col. 2, line 55 – col. 3, line 5, col. 5, lines 27-34, and 57-62 showing the state elements of the model, e.g. the examination of the signals]; and
  - generating a simulation model [5] of the functional design of the logic circuit and a separate (HDL) model of the hardware design of the logic circuit from the data structure [col. 2, line 61 – col. 3, line 5, and col. 5, line 57 – col. 6, line 2; the cited portions are interpreted by examiner to read on the generation of separate models for the simulation and hardware because the views are disclosed by Lee

to be user selected design objects which are separate and are models of the designers choice of components for further design processes];

[2] wherein the data structure comprises a description of a net list [col. 2, line 12-14, ].

[3] wherein the data structure comprises:

elements representing logical functions, connection points to gates, all bits of a simulation state, and an arbitrary collection of bits within the simulation state [col. 3, lines 1-5, col. 5, lines 27-34, col. 5, line 58 – col. 6, lines 8, since the circuit may be simulated in entirety or by portion, the collection of bits of the simulation state are collected in entirety or by portion which reads as all bits and an arbitrary collection of bits of the simulation state].

[7] wherein the HDL is verilog [col. 2, lines 39-42].

[8] wherein the HDL is very high speed IC HDL (VHDL) [col. 2, lines 39-42].

[9] generating a verilog model from the descriptive netlist [cols. 3-4 show the verilog HDL is generated from user selected views];

[11 and 23] the netlist comprises gates, nodes and nets [col. 2, lines 20-27, 40-67, and col. 3].

[19-21] the processor and memory are incorporated into a personal computer, network server, and single board computer[col. 7].

Lee did not specifically generating a C++ (simulation model), and C++ classes.

Art Unit: 2812

Parson disclosed generating C++ models and c++ classes [col. 13, lines 29-67, and col. 14].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Lee and Parson because adding Parson's C++ models and C++ classes would have improved Lee's system for generating models by improving the simulation of Lee's system through the use of conventional language such as C++ which can be linked with commercial simulators and class declarations which require little tuning and can determine the range for signal values that are usable for simulation [see Parson, cols. 13-14]

4. As for claims 15-17, Lee in view of Parson disclosed the invention substantially as claimed, including the computer program product for generating a model as disclosed in the rejection of claims 1 and 14 above.

Lee in view of Parson did not specifically disclose a RAM, ROM or hard disk drive for use in storing the computer program product.

"Official Notice" is taken that both the concepts and advantages of using RAM, ROM, and hard disk drives for the use of storing computer program products (software) are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a RAM, ROM, or hard disk drive for storing Lee in view of Parsons computer program product in order storing the computer program product for execution on the computer system utilized by Lee in view of Parson.

5. Claims 12 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US Patent 6,366,874) in view of Parson (US Patent 6,053,947), and further in view of Anderson (US Patent 6,519,755).

6. As for claims 12 and 24, Lee in view of Parson disclosed the invention substantially as claimed, including the method, system of generating a circuit design wherein the netlist comprises gates and nodes and analyzing the elements as cited above in the rejections of claims 1 and 22.

Lee in view of Parson did not specifically disclose parsing the elements.

Anderson disclosed parsing the elements [col. 5, lines 16; fig. 28; and col. 10, line 55 – col. 11, line 5].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Lee in view of Parson, and Anderson because parsing and analyzing the elements would have improved Lee in view of Parson system by providing a method of representing elements in a word oriented database which would allow for objects to be easily represented as values such as integers which are easier to use than bit oriented constructs [see Anderson, col. 10, line 55 – col. 11, line 5]

7. Claims 13 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US Patent 6,366,874) in view of Parson (US Patent 6,053,947), and further in view of Seawright (US Publication 2002/0023256).

As for claims 13 and 25, Lee in view of Parson disclosed the invention substantially as claimed, including the method and system for code generation as cited above in claims 1, 9, and 22.

Lee in view of Parson did not specifically disclose partitioning a topology of the net list into a plurality of partitions; and code ordering each of the partitions.

Art Unit: 2812

Seawright disclosed partitioning a topology of the net list into a plurality of partitions; and code ordering each of the partitions [fig.'s 4-5; pg. 3-4, paragraphs 45-51].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Lee in view of Parson, and Seawright because Lee in view of Parson, and Seawright all disclose the circuit design using hardware descriptions which would benefit by Seawright partitioning and code ordering of the netlist topology because Seawright's partitioning process optimizes the hardware description which would improve design and Seawright code ordering (recoding) the partitions would be necessary for recoding the optimized hardware descriptions.

8. Applicant's arguments with respect to claims 1-5, 7-9, and 11-25 have been considered but are moot in view of the new ground(s) of rejection.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A Whitmore whose telephone number (571) 272-

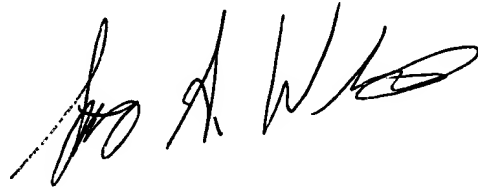
1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is (703) 305-3719.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Stacy A Whitmore  
Primary Examiner  
Art Unit 2812

SAW

A handwritten signature in black ink, appearing to read 'Stacy A. Whitmore', with a stylized, cursive script.